REMARKS

Reconsideration and allowance are respectfully requested.

Applicants appreciate the Examiner's indication of allowable subject matter. With respect to the Examiner's reasons for allowance, Applicants agree that the combination of features recited in these claims is patentable. To the extent that the Examiner's reasons for allowance/allowability are inconsistent with or add additional limitations to the claims, Applicants respectfully disagree because the claims define the invention.

Claims 17-21 and 28-30 stand rejected for indefiniteness under 35 U.S.C. §112, second paragraph. Specifically, the Examiner contends that the language from claim 17, " if said first clock signal is at a second level when said switching signal is received, said processor clock control device is operable to hold said clock signal output at said second level, and then to sense said second clock signal and when said second clock signal transitions from a first level to said second level to output said second clock signal," inaccurately describes Figure 3B(iii). Applicants respectfully request reconsideration.

Claim 17 states that the processor clock control device is responsive to a received switching signal. Turning to the non-limiting example of Figure 3, the received switching signal may be read on the synchronized switching signal of Figure 3. In this non-limiting example embodiment, the switching signal is passed to the clock switching device when REFCLK goes high, whereupon it is passed as a synchronized switching signal. It is this synchronized switching signal that the circuit receives and responds to. And it is the processor's response to this signal that is claimed (for this non-limiting example). In the switching shown, after the synchronized switching signal is received, the first clock is held at the low level (either immediately or once it transitions to it) and then when the second clock transitions from high to

low, the output clocks are switched. For the synchronized switching signal (in this example, see page 8, line 18), this is the switching signal sent when the reference clock is high. Further details of this example are recited in dependent claims 26 and 27. Similar reasoning applies for claim 29. Thus, claims 17 and 29 may be read compatibly with Figure 3B (iii).

The antecedent basis issue noted for "said first predetermined level" in claim 28 has been remedied by amendment.

Withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

The application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

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